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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,544	11/21/2001	Chung-Shi Liu	67,200-535	4986

7590 10/09/2003

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EXAMINER	
LEADER, WILLIAM T	

ART UNIT	PAPER NUMBER
1742	2

DATE MAILED: 10/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,544	LIU ET AL.	
	Examiner	Art Unit	
	William T. Leader	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 11 recites the limitation "said conductive area" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-5, 7-16 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Landau (6,261,433) in view of Palagonia (5,907,785) and Romankiw (6,596,624).

6. The Landau patent is directed to a process for electrochemical deposition of a metal onto a semiconductor wafer. The wafer would have a central portion and a peripheral portion. The basic steps for the deposition of a metal are shown in figures 1A to 1E which are a cross sectional diagram of a layered structure 10. Insulting layer 16 of a dielectric material is formed on an underlying layer 14 which contains electrically conducting features 15. Dielectric layer 16 is patterned and etched to form a dual damascene vias and trenches. Each via has a floor 30 exposing a small portion of the conducting feature 15. See column 2, lines 33-48. These steps correspond to the limitations recited in lines 4-9 of claim 1. A barrier layer 20 of tantalum or tantalum nitride is deposited. Then copper seed layer 21 is deposited. This corresponds to the seed layer recited in line 10 of claim 1. The formation of the metallization structures occurs across the width of the wafer. The via openings adjacent the periphery of the wafer may be considered to correspond to the cathode contact area etched openings recited in claim 1, line 14. As noted above, the underlying conductive features are exposed at the bottom of the vias.

The seed layer which lines the walls and bottom of the vias is in electrical communication with the underlying conductive feature. This corresponds to the limitation in claim 1, lines 15-16. Landau discloses that the vias are filled with electroplated copper (column 3, lines 17-19). This corresponds to the step recited in claim 1, lines 17-19. The top portion of the structure 10 is planarized, preferably by chemical-mechanical polishing (column 3, lines 20-26). This corresponds to the step recited in claim 1, lines 20-21. The steps recited in instant claim 11 are similar to those recited in claim 1.

7. Claim 1 differs from the process of Landau by reciting the formation of a conductive layer over the metal interconnects to form contact pads. The Palagonia patent is directed to the production of a semiconductor wafer with elevated contact substructures. The contacts allow the chip to be connected to other components. The raised contact pads are formed at wafer level using existing methods of photolithography (column 2, lines 28-31. Wafer 20, on which the contacts are formed, is made up of a semiconductor substrate material which is processed with conductive and insulative materials to form integrated circuits embedded within the substrate (column 3, lines 8-12). Typically, a complete integrated circuit pattern will be replicated a number of times on wafer 20 (column 3, lines 13-16). This is illustrated in figures 1a and 1b and corresponds to the wafer of Landau.

8. The Romankiw patent (6,596,624) is directed to the production of integrated circuit structures. As shown in figure 2C, the circuit includes multiple layers of metallized vias and trenches formed in insulating layers. This corresponds to the metallization structures of Landau. Conductive vias ultimately terminate at contact pads 4 (column 6, lines 46-47).

9. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have form contact pads on the metallization of Landau so that the integrated circuits could be connected to other components as taught by Palagonia and Romankiw. It is noted that applicant's specification discloses that the cathode contact areas may be formed in parallel with active device area features in the central portion of the semiconductor wafer (page 23, lines 1-3). There appears to be no distinction between the cathode contact areas and the active device area features and the process steps used to form them other than the recitation that they are within the peripheral portion of the semiconductor wafer (claim 1, lines 11-12). However, Palagonia shows that device features extend to the peripheral portion of the wafer.

10. With respect to claims 2 and 12, Landau discloses the formation of barrier layer 20 which covers the sidewalls and floors of the etched openings as shown in figure 1B. With respect to claims 3 and 13, Landau teaches that the barrier layer may be made of tantalum or tantalum nitride (column 2, lines 58-59). With respect

to claims 4 and 14, Landau discloses that the deposited metal may be copper (column 3, lines 10-15). Landau uses a dual damascene process for forming the interconnect features (column 2, lines 19-23) and, as shown in figures 1A-1E of Landau, this includes the formation of vias and trenches as recited in claims 5, 15 and 16. As noted above, Romankiw shows the formation of contact pates 4 above the metallization layers. Choice of an appropriate size of contact pad, such as that recited in claims 7 and 18, to allow connection to other circuit elements is a matter of optimization within the skill of the ordinary worker in the art, recognizing that the contact must be large enough to conduct the desired current but not so large as to excessive surface area of the wafer. Landau teaches that the contacts should touch the seed layer as close as practically possible to the edge of the substrate, to minimize the wasted area on the wafer due to the presence of the contacts (column 3, lines 48-51). This suggests the limitations of claims 8, 9 and 19. As shown in Palagonia, devices are formed around the entire periphery of the wafer suggesting the limitation of claim 10. The metallization takes place across the surface of the wafer including the central portion to form a plurality of integrated circuits as shown in Palagonia, suggesting the limitation of claim 20.

11. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Landau (6,261,433) in view of Palagonia (5,907,785) and Romankiw (6,596,624)

as applied to claims 1-5, 7-16 and 18-20 above, and further in view of Krishnamoorthy et al (6,319,387).

12. Claims 6 and 17 additionally differ from the method of Landau by reciting an insulating layer with a dielectric constant of less than about 3.0. The Krishnamoorthy et al patent is directed to the metallization of semiconductor wafer having small surface features. A parameter of interest in fabricating semiconductor devices is the signal propagation delay. The equation is given at column 1, line 60. In this equation C is the equivalent capacitance for the interconnect path. It is desirable to utilize a low-K dielectric material to minimize capacitance (column 2, lines 5-16). It would have been obvious at the time the invention was made to have utilized a low-K dielectric material in the process of Landau as taught by Krishnamoorthy et al because capacitance, and consequently signal delay, would have been reduced. Based on the formula and teaching of Krishnamoorthy et al, one of ordinary skill in the art would recognize that an insulating layer with as low dielectric constant as possible is desirable and could choose an appropriate value.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 703-308-2530. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 703-308-1146. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

William Leader
September 26, 2003